

REMARKS

The application has been carefully reviewed in light of the Office Action mailed November 14, 2003. Applicant gratefully acknowledges the Examiner's statement that claims 8-12, 15, 16, 20, 21, 30-34, 37, 38, 42, 43, 47, 48, 52 and 53 contain allowable subject matter. Claims 1, 13, 23, 35, 45 and 55-58 have been amended. Claim 25 has been cancelled. Claims 1, 4-23 and 26-58 are now pending in this case.

Claims 1, 4-7, 13, 14, 17-19, 22, 23, 25-29, 35, 36, 39-41, 44-46, 49-51 and 54-58 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Leung et al. (U.S. Patent No. 5,999,474). Applicant respectfully traverses the rejection and requests reconsideration.

Claim 25 has been cancelled; and, therefore, the rejection is no longer applicable to claim 25.

Amended claims 1 and 23 respectively recite a method for refreshing memory cells and a memory device that carries out that method, comprising determining that a data access command has been applied to a command/address bus at a first predetermined time slot, "said first predetermined time slot being one of a plurality of predetermined time slots defining the only time slots on said command/address bus during which data access commands may be placed on said command/address bus." [Emphasis added.] Claims 1 and 23 also recite that the refresh is initiated "during a time period between said first predetermined time slot and a second predetermined time slot of said plurality of predetermined time slots without delaying said data access." [Emphasis added.]

Leung, to the contrary, makes no mention of applying data access commands to the command/address bus at such predetermined time slots. Rather, Leung discloses that the control circuit is configured to enable the memory cells to be randomly accessed and in order to achieve such random access without interfering with such access to perform a

refresh, Leung also discloses a multi-bank DRAM memory and a SRAM cache that stores the most recently accessed data, whereby each of the DRAM banks is operated with independent control, thereby enabling parallel refresh operations and read-write access to different banks. Leung at Abstract. Leung makes no mention of applying data access commands to the command/address bus at predetermined time slots as defined by claims 1 and 23. At least for these reasons, claims 1 and 23 are allowable over Leung.

Amended claims 13, 35, 45, 56, 57 and 58 each recite a system for refreshing memory cells, comprising “a communication link for respectively delivering data access commands to [a] DRAM on a plurality of predetermined time slots, said plurality of predetermined time slots defining the only time slots on said communications link during which said data access commands may be placed on said communications link.” At least for the reasons mentioned above in connection with claims 1 and 23, claims 13, 35, 45, 56, 57 and 58 are also allowable over Leung.

Amended claim 55 recites a method for refreshing memory cells, comprising “assigning a plurality of predetermined time slots on a command/address bus defining the only time slots on said command/address bus during which data access commands may be placed on said command/address bus.” Claim 55 also recites performing a non-conflicting refresh operation “during a period of time between a first and a second of said plurality of predetermined time slots.” At least for the reasons mentioned above in connection with claims 1 and 23, claim 55 is also allowable over Leung.

Claims 4-7, 14, 17-19, 22, 26-29, 36, 39-41, 44, 46, 49-51 and 54 depend from claims 1, 13, 23, 35 and 45, and are allowable over Leung at least for those reasons mentioned above and also because Leung fails to teach or suggest the respective inventive combinations defined by claims 4-7, 14, 17-19, 22, 26-29, 36, 39-41, 44, 46, 49-51 and 54.

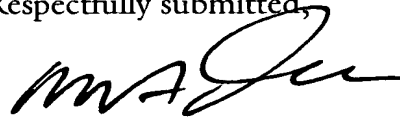
Application No.: 09/641,519

Docket No.: M4065.0290/P290

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejections of the claims and to pass this application to issue.

Dated: February 17, 2004

Respectfully submitted,



By MARK THOMPSON #33,082

Thomas J. D'Amico

Registration No. 28,371

Salvatore P. Tamburo

Registration No. 45,153

DICKSTEIN SHAPIRO MORIN &

OSHINSKY LLP

2101 L Street NW

Washington, DC 20037-1526

(202) 785-9700

Attorneys for Applicant